

## Proposal for solutions for the embedded system exam, 20050110

1 a-e) check either book or lecture slides

2)

```
GLOBAL    F                ; F shall be globally known
                                ; APCS:
                                ;   r0 = a, r1 = b; r2 = c
                                ; local variables:
                                ;   r5 = y, r6 = x, r7 = i

F         STMFID           sp!, {r5-r7}    ; save registers on stack
         MOV              r5, #0          ; y := 0
         CMP              r0, r1          ; a == b?
         MOVEQ            r6, #3          ; yes => x := 3
         MOVNE            r6, #5          ; no => x := 5
         MOV              r7, #1          ; i := 1
FOR       CMP              r7, r6          ; i < x?
         BGE              ENDFOR          ; no => end loop
         ADD              r5, r5, r2      ; yes => y := c + y
         ADD              r7, r7, #1      ; i++
         B                FOR            ; next iteration
ENDFORMOV r0, r5                ; save return value in r0
         LDMFD            sp!, {r5-r7}    ; restore registers
         MOV              pc, lr          ; return to subroutine
```

3)

3. Source File 1

A 0x0

D 0x14

Source File 2

X 0x0

Y 0x4

Z 0x10

Source File 3

num1 0x0

num2 0xc

num3 0x10

2p

b) For each external variable there has to exist an entry in a symbol table that is globally available:

External Variable:

Entry in File (global)

num1 (1)

3

num3 (1)

3

X (1)

2

1p

All external variables have an entry point  $\Rightarrow$  The linker has sufficient info

c) File 1: 6 instructions  $\Rightarrow 6 * 1 = 6$

File 2: (CMP Z, BLE Z  $\Rightarrow 2 * 400 = 800$

SUB ... BX  $\Rightarrow 2 * 399 = 798$

MOV ...  $\Rightarrow 1 * 1 = 1$

1p

Answer 1609 instructions

1605

4)

#### 4. Main Memory (word-addressable)

0    32-bits  
 1    -"-  
 ⋮  
 2043   -"-

##### a. Direct-Mapped Cache

##### Block

0	Word 0	Word 1	Word 2	Word 3	(0,1,2,3) (B)
1	Word 5	Word 6	Word 7	Word 8	(4,5,6,7) (C)

##### i. Mapping

Tag	Block	Offset	
┌───┐	┌───┐	┌───┐	
8	1	2	1p

##### ii. Cache Contents

0x1 =	00000000	0001
	Tag	8 Offset
0x2 =	00000000	0000
0x1A =	00000011	010
0x2F =	00000101	111
0x1B =	00000011	011
0x6C =	00001101	100
0x01 =	00000000	001
0x00 =	00000000	000

⇒ Memory Access	Block	1st Run	2nd Run
0x1	0	Miss	Hit
0x2	0	Hit	Hit
0x1A	0	Miss	Miss
0x2F	1	Miss	Miss
0x1B	0	Hit	Hit
0x6C	1	Miss	Miss
0x02	0	Miss	Miss
0x00	0	Hit	Hit
		3/8	4/8

### Cache Contents

Block	Tag	Word 0	Word 1	Word 2	Word 3
0	0x00	[0x00]	[0x01]	[0x02]	[0x03]
1	0x0D	[0x6C]	[0x6D]	[0x6E]	[0x6F]

3p

### iii Hit Rate:

$$HR = \frac{1}{5} \cdot \frac{3}{8} + \frac{4}{5} \cdot \frac{4}{8} = \frac{19}{40} \quad 1p$$

b). Fully-set associative cache with one word per block cache line can achieve a hit rate of almost 100%

0x00	0x01	0x02	0x1A	0x1B	0x2F	0x6C	...
------	------	------	------	------	------	------	-----

Hit Rate:			
0x1	M	H	
0x2	M	H	
0x1A	M	H	
0x2F	M	H	
0x1B	M	H	
0x6C	M	H	
0x02	H	H	
0x00	M	H	

$$HR = \frac{1}{5} \cdot \frac{1}{8} + \frac{4}{5} \cdot \frac{8}{8} = \frac{33}{40} = 82,5\% \quad 3p$$

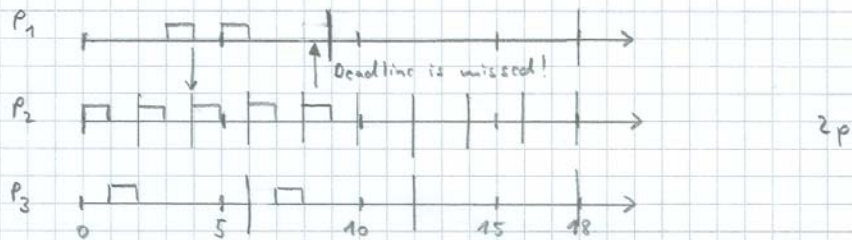
5)

5.

a)  $U = \frac{3}{9} + \frac{1}{2} + \frac{1}{6} = 1$  1p

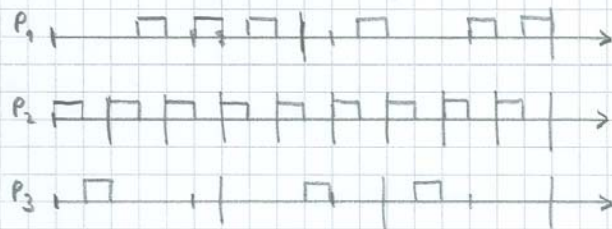
b) RMS schedule is not guaranteed, since  $U > 3(2^{1/3} - 1) \approx 0,78$ , but there may still be a feasible schedule!

Priority:  $P_2 > P_3 > P_1$  1p



No feasible schedule!

c) EDF schedule exists, if  $U \leq 1$ !



Feasible schedule exists!

2p